(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 01/69679 A1

(51) International Patent Classification[7]: H01L 23/522, 21/60

(21) International Application Number: PCT/NO01/00113

(22) International Filing Date: 15 March 2001 (15.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20001360 15 March 2000 (15.03.2000) NO

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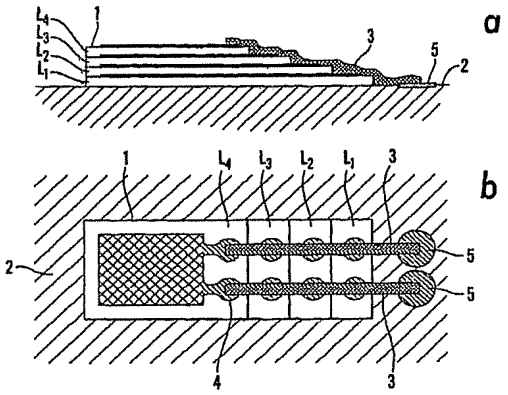
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK



(57) Abstract: In a memory and/or data processing device having at least two stacked layers which are supported by a substrate or forming a sandwich self-supporting structure, wherein the layers comprise memory and/or processing circuitry with mutual connections between the layers and/or to circuitry in the substrate, the layers are mutually arranged such that contiguous layers form a staggered structure on at least one edge of the device and at least one electrical edge conductor is provided passing over the edge on one layer and down one step at a time, enabling the connection to an electrical conductor in any of the following layers in the stack. A method for manufacturing a device of this kind comprises steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

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Vertical electrical interconnections in a stack

The present invention concerns a memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or substrate; and a method for manufacturing a device of this kind.

Modern electronic microcircuits are typically built layer by layer on silicon chips in a series of process steps where insulating layers separate layers containing metallic, insulating and semiconducting materials that are patterned and processed by various deposition and etching techniques. Integral to the ensuing architectures are electrical connections between components and sub-circuits which are located in the substrate and in layers on top of the substrate. These connections, termed vias, are typically in the form of metallic posts or wires that penetrate through one or more layers of intervening material separating the components to be connected. Such vias are either made during the layer-building process or they are inserted through already existing layers by creating channels through the layers (by e.g. etching), followed by filling metal plugs into the channels.

Present-day state-of-the-art silicon chips may involve 20-30 masking steps, and the number of separate layers containing patterned metal intra-layer leads that connect directly or indirectly to a via is typically 3-5. Each via requires a certain amount of real estate associated with it in each layer that is traversed or connected: In addition to the metal cross section of the via itself, there must be allocated a buffer zone around it which insulates the via from adjacent circuitry that shall not be in immediate contact with the via, and allowance must be made for the finite precision with which the patterning in each layer can be made as well as registration accuracy of patterning masks.

The above referred prior art has generally proved adequate for devices built on silicon substrates as referred above, where the number of layers and vias is low to moderate, and where ultra-high precision lithography is an integral part of the chip-making process. However, vias represent a considerable complicating feature in the overall manufacturing process, with impact on

yield and costs. Furthermore, it is expected that entirely new types of device architectures and manufacturing methods for electronic data processing and -storage shall emerge in the next few years as serious contenders for large commercial segments. A common feature of such new architectures shall be that they incorporate thin-film electronics in dense stacks containing very large numbers of layers. In many instances, these devices shall be manufactured by high-volume technologies such as roll-to-roll processing on thin polymer substrates. In this context, traditional via connection technologies shall be totally inadequate, technically as well as cost-wise.

It is a major object of the present invention to provide methods and technical solutions whereby electrical interconnects can be created between layers and/or between layers and an underlying substrate, in memory and/or processing devices that incorporate a stack containing two or more sheet- or film-like functional parts that partially or completely overlap each other.

It is also an object of the present invention to provide such methods and technical solutions that can be implemented in cases where the number of such sheet- or film-like functional parts becomes large, typically exceeding 5-10.

It is a further object of the present invention to provide such methods and technical solutions that can be implemented in cases where such sheet- or film-like functional parts are manufactured and devices assembled by high-volume, low cost technologies.

The above-mentioned objects and further features and advantages are realized according to the invention with a device which is characterized in that said layers are arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said structure forming a set of angular or sloped steps where each step has a height corresponding to the thickness of each layer, and that at least one electrical edge conductor is provided passing over the edge of one layer and down one step at a time, enabling the connection to an electrical conductor in any of the layers following in the staggered structure; and a method which is characterized by comprising steps for adding said layers successively, one layer at a time such that the layers form a staggered structure, and for providing each layer with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

In an advantageous embodiment of the device according to the invention comprises at least one electrical conductor provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.

In this connection it is preferred that said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.

In a first advantageous embodiment of the method according to the invention said layers are provided on a supporting substrate and forming said staggered structure is formed as a step pyramid.

In a second advantageous embodiment of the method said layers are provided on a supporting substrate, said staggered structure is formed as an inverted pyramid, each of said layers connecting to said substrate via said electrical edge connectors negotiating a single step.

Finally, in the method according to the invention it is considered advantageous forming said edge connectors in a process selected among one of the following, viz. lithography, dry etching, inkjet printing, silk screen printing, soft lithography, electrolysis, or in situ conversion

The invention shall now be described in detail, with reference to the accompanying drawings, where

fig.1a shows a side view of a generic device, termed of the "pyramid" type here. It consists of stacked functional units located on separate but mutually adhering sheets or film layers mounted on a base substrate. Circuitry on the top surface of a given layer is electrically connected to localized contacting pads on an exposed edge area of that sheet.

Figs. 1b and 1c show top views of two alternative architectures consistent with the side view in Fig.1a. In Fig.1b the structure is stepped in one direction, in Fig.1c in two.

Fig.2 shows an analogous structure to that shown in Fig.1a, but now the edge of each layer is sloped or tapered

Fig.3 shows an analogous structure to that shown in Fig.1c, buit now multiple contacting pads are provided on each step, yielding possibilities for patching of intra- and inter-layer connections.

Figs.4a-c show analogous structures to those in Fig.1a, but in this case the stack is self-supporting, i.e. there is no supporting substrate.

Fig.4d also shows a self-supporting structure. In this case both sides of each layer can be accessed separately.

Figs.5a-e show an example of manufacturing steps for creating structures of the type shown in Fig.1a.

Figs.6a-d illustrate an alternative example to that in Figs.5a-e of manufacturing steps for creating structures of the type shown in Fig.1a. In this case, edge connections are made one step at a time, to conform with e.g. limited depth of field when employing high resolution optical lithography in making of the edge connections.

Fig.7 shows a side view of a generic device, termed of the "inverted pyramid" type here. As with the pyramid type devices, it consists of stacked functional units located on separate but mutually adhering sheets mounted on a base substrate. In this case, however, the area of each layer in the stack increases as the distance from the substrate increases. Each layer has its separate access to dedicated landing pads in/on the substrate.

Figs.8a-g show an example of manufacturing sequence for creating structures of the type shown in Fig.7.

Figs.9a-b show, for the "pyramid" and "inverted pyramid" case, respectively, how patterning of connectors across a stack edge can be achieved with moderate depth of field requirements and correspondingly high resolution, by patterning at an oblique angle to the planes of the layers in the stack.

Fig. 10 shows a prior art passive matrix arrangment.

Fig.11a-m shows an example of manufacturing steps in making a stacked, passive matrix addressed memory. For simplicity, the device shown has only 2 word-lines, 3 bit-lines and 3 memory layers.

According to the present invention, electrical connections between layers in a stack and/or between such layers and a supporting substrate are created by negotiating a stepped or sloped edge of the stack, as shown schematically in figs. 1a-c.

Fig.1a shows a side view of a stack, where common connector provides electrical contact between an exposed contact pad in the substrate and exposed conductors on the steps of the stack.

Fig.1b shows a top view of the stack in fig.1a, with exposed contacting pads in each given layer being linked electrically by in-layer conductors to specific parts of the circuitry in that layer. In the figure, the circuitry in the top layer is shown as a cross-hatched field. The latter may of course represent one or more networks of physically separated components or circuits, and the two connecting paths to the substrate shown in the figure couple to different parts of the in-layer circuitry.

Fig.1c shows a top view of a different stack which also is compatible with the side view in fig.1a. In this case, the stack is stepped in two mutually orthogonal directions, providing increased exposed step area for coupling purposes as well as spreading out the contacting pad locations on the substrate. Clearly, a number of alternatively stepped structures in 3, 4, 5 etc. directions are possible by direct extension of the principles described here.

In order to reduce the risk of breaking the electrical continuity at the point where the connector climbs a given step, that step may be rounded at the edge, or shaped as a gradual slope, cf. fig. 2.

The generic edge connectivity shown in figs. 1 and 2 may be achieved either in a single electrode deposition step (cf. fig. 5e) or in a sequence of deposition operations (cf. fig. 6b-d). In the latter case, each deposition operation involves negotiating a smaller part of the total edge height, e.g. a single step in the edge structure, and continuity of the electrical connection across several steps is achieved by overlap between successively deposited electrodes.

Each layer in the stack may itself be a sandwich of sub-layers containing electrical conduits, active circuitry and functional materials, e.g. memory substances for data storage purposes. Depending on the chosen technologies, each layer may be prefabricated on a supporting film member before being built into the stack, or it may be constructed by one or a series of deposition processes onto the surface of the stack itself. In the former case, each layer may have a thickness whose lower limit shall be defined by the structural strength of the supporting film in relation to the stress it is subjected to during the prefabrication and stack addition processes. In the latter case, the layer thickness may be much less, down to monolayer coverages.

Although it is possible to combine the principles of the present invention with prior art-type penetrating vias, one should note certain salient features which set the two qualitatively apart:

- In the present invention, vertical connectivity in the stack as well as intra-layer patching can be achieved in manufacturing operations after the layers in the stack have been laid down, providing increased flexibility in selecting manufacturing strategies (materials compatibility issues; customizing of devices, e.g. post stacking).

- In the present invention, no etching, drilling or similar operation is required to open connecting channels through layers in the stack.

- The present invention provides realistic routes towards large-scale manufacturing of stacked devices in low-cost, high-volume operations such as roll-to-roll production of polymer-based devices.

As thin-film based active circuitry employing inorganics, oligomers or polymers enters the mainstream of commercial electronics, it is expected that stacked devices with "smart" layers, i.e. layers that possess individual processing capabilities, shall become ubiquitous. In addition to enhancing the possibilities inherent in the stacking concept, this implies that bus-type edge connections may carry messages that are distributed globally across the stack and picked up selectively by those layers they are intended for. On the other hand, the interconnect concepts of the present invention may involve stacks that contain sheets or layers without decoding circuitry, in which case dedicated edge connections to those sheets may have to be provided. An extreme case of the latter is where all layers are "dumb" and where each

layer has dedicated electrical connections to driving circuitry on a supporting substrate or circuitry at a cable-connected location elsewhere. In what follows, these different aspects of possible electronic capabilities in individual layers shall not be treated in any further detail, since the appropriate choices of solutions according to the present invention will be obvious to the skilled person.

Before turning to more detailed discussions related to preferred embodiments, certain generic aspects of the present invention shall be pointed out:

Examples of these are shown in figs.1, 2 and 3. The edge connections on a given layer in a stack are established by allocating an edge area of that layer for contacting purposes, the layers in the stack being mutually arranged in a series of steps. The stack may be stepped in one direction only, as shown in fig. 1b, or it may be stepped in two or more directions (cf., e.g. fig. 1c). These steps are exposed during the manufacturing of contacts, but may subsequently be protected by coating, etc.

Application of inter-layer and/or layer-to-substrate contact lines may be performed by a range of techniques, ranging from high-volume, low-cost to precision, high-cost. If precision is less important than cost, printing techniques may be preferred (ink-jet, silk screen, stamping, electrostatic deposition), with the proviso that the edge conductors thus created must be able to negotiate the steps in the stack. In high-density devices, edge connectors must be defined with high precision, not only where they shall connect to a small contacting area on the step of a given layer, but also where they climb the edge of the stack and shall encroach as little as possible to each side. Thus, a single edge of a stack may well contain hundreds or thousands of parallel conductors climbing up the side (for practical reasons, only a single or a few conducting lines are shown in the figures here).

Techniques for creating edge connectors with high precision include lithographic techniques with wet or dry etching, as well as particle milling, high precision stamping such as "soft lithography" and electrolysis. Common to most high resolution techniques is a restricted depth of field, limiting the height of each step and/or the number of steps that can be bridged electrically in a single manufacturing step. In such cases, a single application of a

common conductor (power; bus...) may be employed as shown in fig. 5, where:

Fig. 5a shows the substrate before building of the stack, with a circuit connecting to contacting pads.

Fig. 5b shows how an insulating layer masks off the parts of the substrate that might interfere chemically or electrically with the stack, leaving the contacting pads exposed. A first-layer circuit has been applied onto the insulating layer, with contacting pads near the edge.

Fig. 5c shows the situation following application of a second insulating layer and subsequent circuitry with connecting pads near the edge.

Fig. 5d shows the stack after application of a third insulating layer and circuitry, with exposed contact pads arranged in a sequence along the staircase edge.

Fig. 5e shows how a conducting line has been applied along each row of connecting pads on the steps, linking these pads to the connecting pads in the substrate.

The single-step application of inter-layer and layer-substrate connections can be supplanted by a stepwise approach as shown in figs. 6a-d:

Fig. 6a shows a substrate with circuitry and connecting pads, in analogy with Fig.5a.

Fig. 6b shows how an insulating layer has been applied, with circuitry and connecting pads on top.

Fig. 6c shows how an electrical connection has been established between connecting pads in the substrate and corresponding ones at the edge of the first layer in the stack.

Fig. 6c shows the situation after a second insulator layer with circuitry on top has been applied, the latter being connected via connecting pads to the exposed conductors on the step below.

Fig. 6d likewise shows how a third layer in the stack has been established, with electrical links to the layer below and thence to the substrate.

In this way, only the height of each step is negotiated in each contacting operation, which can be repeated ad libitum to achieve any desired total stack height. An alternative approach is illustrated in figs. 9a-b: Here, the steps on a side of the stack are arranged so as to present a linear slope. As can be seen, the required depth of field for application of conductors spanning the whole height of the stack can be made very small by attacking the edge at an oblique angle. A regular step height is not required, cf. fig. 9a.

In order to maximize the usable area of the layers in the stack, the area on any given layer occupied by the exposed part of the step should be kept small, but this must be weighed against the ease of manufacturing the device: A shallow step imposes closer tolerances on the contacting procedures, and steepens the edge slope of the stack. The latter aspect may prove negative in certain cases where it is desired to create edge connections by application of conductors at a skew angle (cf. references to figs. 9a-b, above). In the limiting case where steps become infinitely shallow, the stack shall have a straight edge, and circuitry in a given layer must then be accessed by electrical wiring that extends to the edge of that layer and provides exposed electrical contact material laterally from that edge.

Please refer to fig. 7. In this case, the stack is built layer by layer on a substrate which provides physical support and has on its surface electrical contacting areas as shown. Each subsequent layer extends beyond the previous one at the stepped edge, typically causing the total area of each layer to increase with the distance from the substrate. In addition to providing each layer with direct access to possible driving circuitry in the substrate, as can be the case when the substrate is a chip of silicon, electrical conduits in the substrate may connect separate layers in the stack electrically to each other via the contacting pads shown.

An example of a manufacturing sequence for a stack of the inverted pyramid type is shown in figs. 8a-g, wherein specifically

fig. 8a a substrate with connecting pads,

fig. 8b how an insulating layer has been added, masking the part of the substrate to be covered by the stack, but leaving the contacting pads exposed,

fig. 8c the situationafter application of a set of electrodes in the first stack layer connecting to the first row of contacting pads on the substrate,

fig. 8d how a second insulating layer masks off the first-layer electrodes, leaving the second-layer and subsequent-layer electrodes exposed on the substrate,

fig. 8e how a second-layer set of electrodes have been applied, climbing up two steps from the connecting pads on the substrate,

fig. 8f the situation after a third insulating layer has been applied, leaving the third-layer connecting pads in the substrate exposed, and

fig. 8g finally how a set of electrodes has been applied, providing electrical connections to the appropriate connecting pads in the substrate.

As can be observed, the latter procedure provides separate access to individual layers in the stack, as opposed to the example shown in Figs. 5 and 6.

As illustrated in figs. 4a-d, stacks may be formed without a supporting substrate, having properties that can be deduced by trivial extension of those discussed in connection with the substrate based variants above. A special aspect of self-supporting structures is increased access to exposed edges, providing opportunities for two-sided contacting as illustrated in fig. 4d.

A passive matrix arrangement is shown in fig.10: It provides a simple, dense architecture for providing addressed cells located at the crossing points between the word lines and the bit lines, and has been used in applications that include memory devices and displays.

For concreteness, the present example of a preferred embodiment shall focus on the case of memory devices, but the general principles shall be applicable to other types of devices also:

The crossing electrodes sandwich a global layer of memory material, a memory cell being formed in the volume between each crossing of a word- and a bit-line. A given cell can be written to, read and erased by activating the word- and bit-line electrodes crossing at that cell (in fig. 10, the activated lines are shown in a darker shade). A memory matrix containing a sheet of memory material sandwiched between word- and bit-lines may contain hundreds or thousands of such lines in each direction and extend laterally across macroscopic distances (millimeters to centimeters). The thickness of this structure, however, is typically very small, of the order of a micrometer

and less. By stacking such matrices on top of each other in a monolithic structure where each layer containing a matrix is insulated electrically against cross-talk interference from other layers in the stack, extremely high volumetric densities of memory cells can be achieved.

In a high-density stack of large matrices, the number of matrix lines in the device that must be connected to appropriate driving circuitry shall be very large. If the layers in the stack are passive, with all active circuitry for switching , multiplexing, sensing or processing located in the supporting substrate, the number of direct electrical connections between individual layers in the stack and the substrate may become comparable to the total number of matrix lines in the device, and manufacturing issues shall be of paramount importance.

Fig. 11a-m shows an example of how a dense stack of passive matrix devices can be manufactured in a series of manufacturing steps providing high density electrical connectivity to the substrate. In this example, corresponding wordlines in separate layers are connected to a common conductor, while a separate set of bit-lines is provided for each layer.

Fig. 11a shows the substrate prior to deposition of the stack, with contacting pads exposed.

Fig. 11b shows the substrate with an insulating layer to protect against electrical or chemical interference between substrate and stack.

Fig. 11c shows how bit-lines for the first layer in the stack have been laid out, connecting to the first row of bit-line connecting pads in the substrate.

Fig. 11d shows how a film of functional material, in this case a film with memory capability, has been deposited on top of the bit-lines.

Fig. 11e shows how the word-lines have been laid out, connecting to the row of word-line connecting pads in the substrate.

Fig. 11f shows the situation after an insulating layer has been applied, masking off the first row of bit-line connecting pads in the substrate and completing the first memory device in the stack.

Fig. 11g shows how the bit-lines of the second memory device have been applied so as to connect to the second row of bit-line pads in the substrate.

Fig. 11h shows how the film with memory capability has been applied on top of the bit-lines.

Fig. 11i shows how the word-lines have been applied, and connected to the exposed word-line segments in the layer below, thereby achieving contact to the contacting pads in the substrate.

Fig. 11j shows how an insulating film has been applied, masking off the second row of bit-line connecting pads in the substrate.

Fig. 11k shows how the complement of bit-lines in the third memory matrix of the stack have been applied, connecting to the third row of bit-line connecting pads in the substrate.

Fig. 11 l shows how the film with memory capability has been applied on top of the bit-lines.

Fig. 11m shows finally how the third memory matrix device in the stack is supplied with bit-lines that are connected to the exposed word-line segments in a layer below, providing electrical contact down to the word-line contacting pads in the substrate.

As will be apparent, the above detailed description of manufacturing steps represents but one amongst several alternative procedures according to the present invention that can be employed to create a stacked series of memory matrices. Thus, it might be preferable in certain instances to create the word-line in a single step, by procedures analogous to those shown in figs. 5a-e. Likewise, the application of bit-lines as shown in fig.11k implies that a number of layers must negotiated in a single manufacturing step. If this represents a problem, alternatives exist such as illustrated in fig.9b, or sequential connections with patching to a lower step may be used in analogy with that shown in figs. 6a-d.

PATENT CLAIMS

1. A memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or said substrate,
characterized in that
said layers are arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said structure forming a set of angular or sloped steps where each step has a height corresponding to the thickness of each layer, and that
at least one electrical edge conductor is provided passing over the edge of one layer and down one step at a time enabling the connection to an electrical conductor in any of the layers following in the staggered structure.

2. A memory and/or data processing device according to claim 1, characterized in that said
at least one electrical conductor is provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.

3. A memory and/or data processing device according to claim 2, characterized in that
said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.

4. A method for manufacturing a memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or substrate, and wherein the method is

characterized by
comprising steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

5. A method according to claim 4,
characterized by providing said layers on a supporting substrate, and forming said staggered structure as a step pyramid.

6. A method according to claim 4,
characterized by
providing said layers on a supporting substrate and forming said staggered structure as an inverted pyramid, each of said layers connecting to said substrate via said electrical edge connectors negotiating a single step.

7. A method according to claim 4,
characterized by
forming said edge connectors in a process selected among one of the following, viz. lithography, dry etching, inkjet printing, silk screen printing, soft lithography, electrolysis, electrostatic deposition, or in situ conversion.

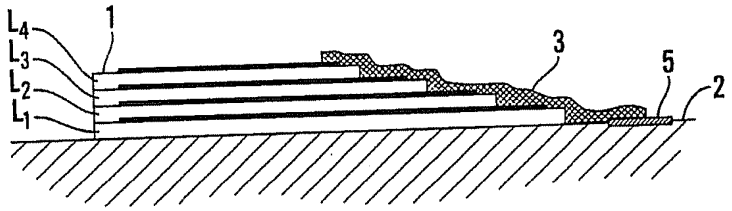


Fig.1a

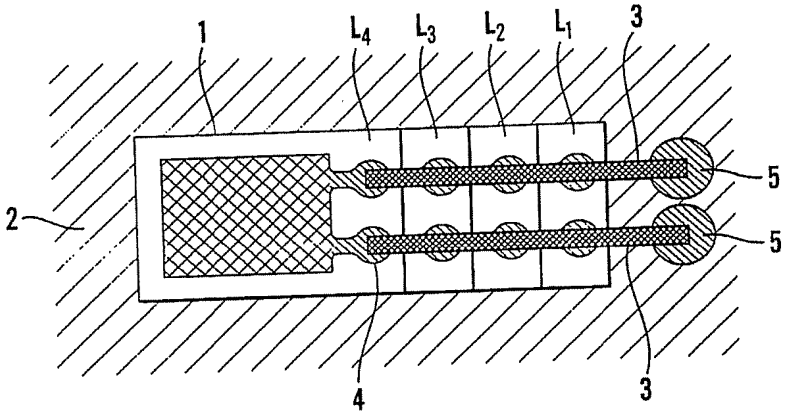


Fig.1b

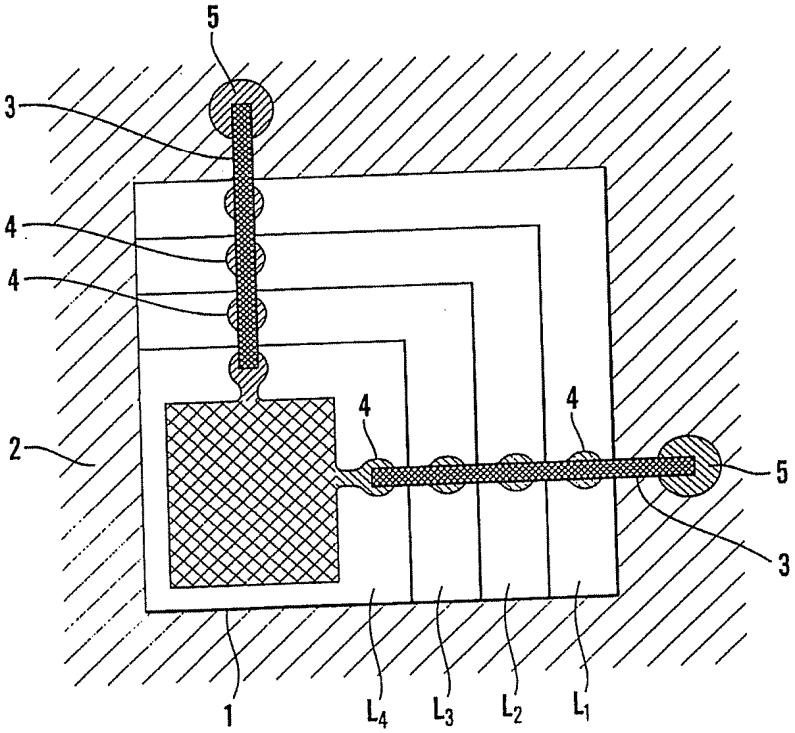


Fig.1c

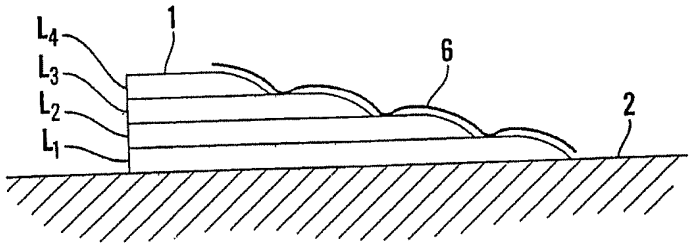


Fig.2

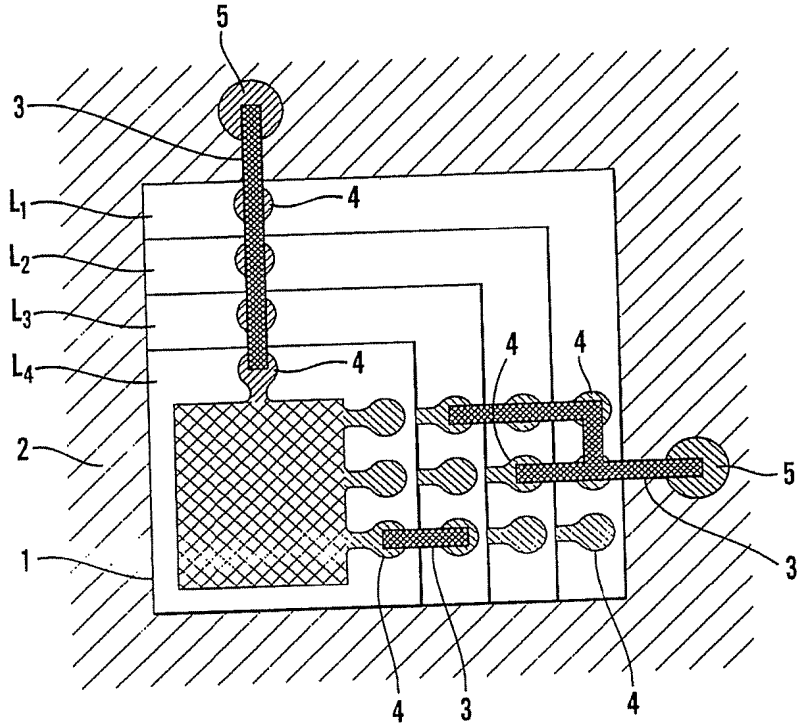


Fig.3

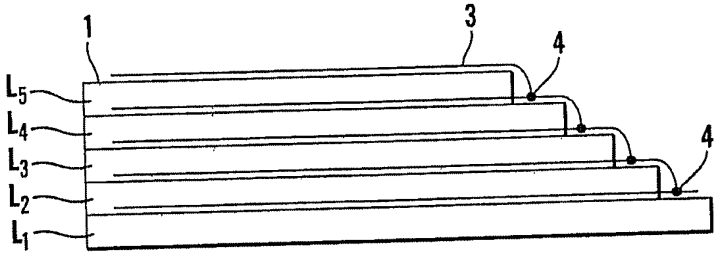


Fig.4a

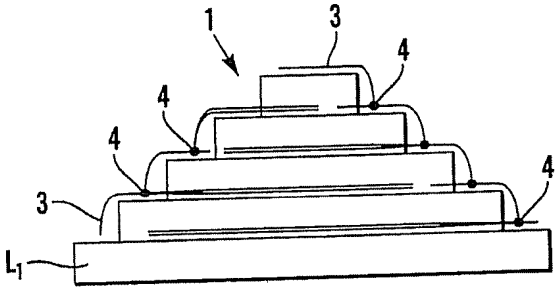


Fig.4b

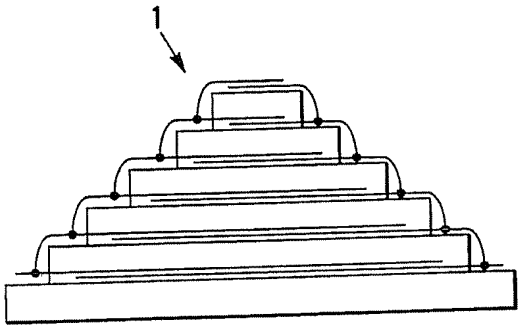


Fig.4c

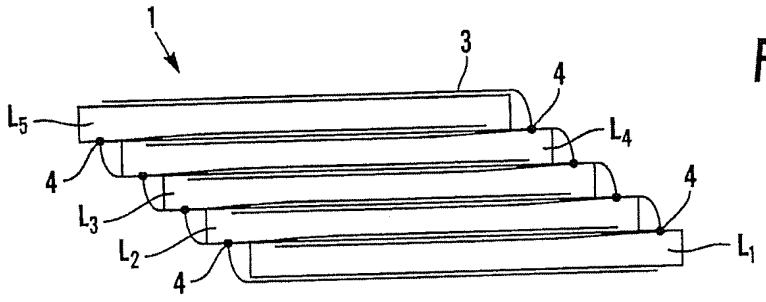


Fig.4d

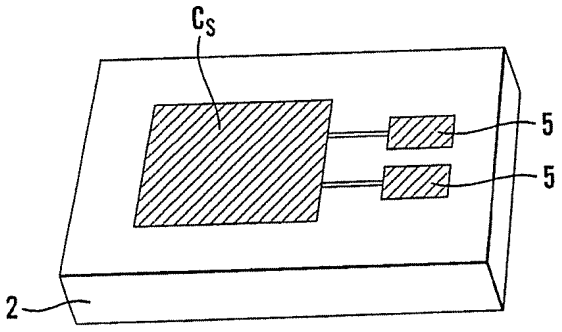


Fig.5a

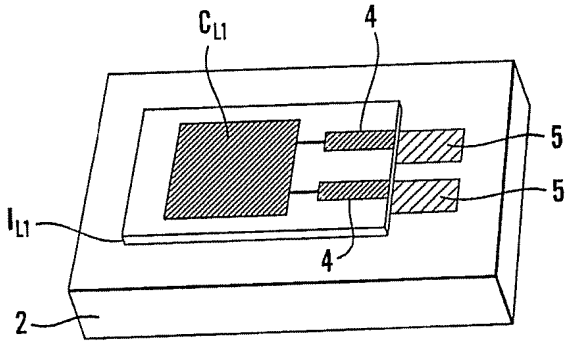


Fig.5b

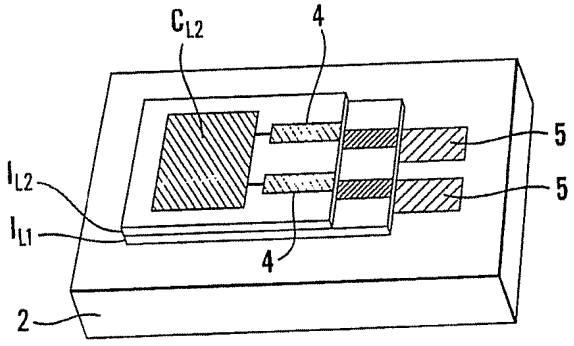


Fig.5c

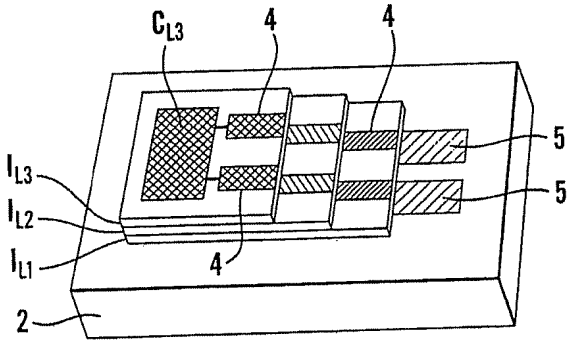


Fig.5d

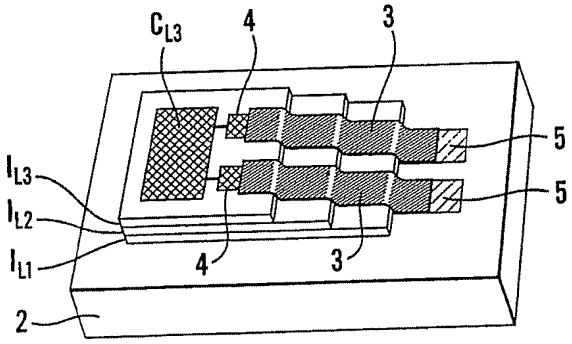


Fig.5e

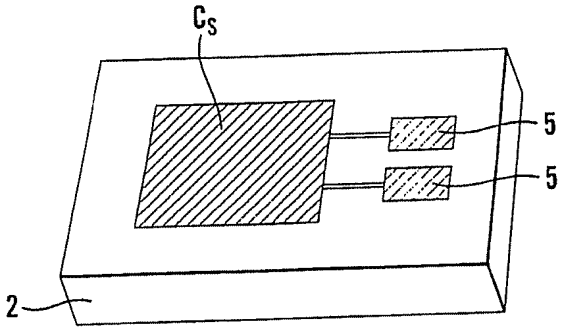


Fig.6a

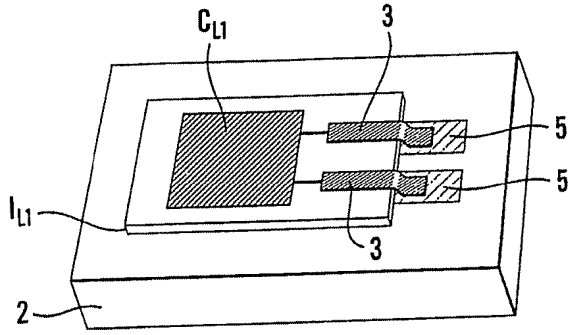


Fig.6b

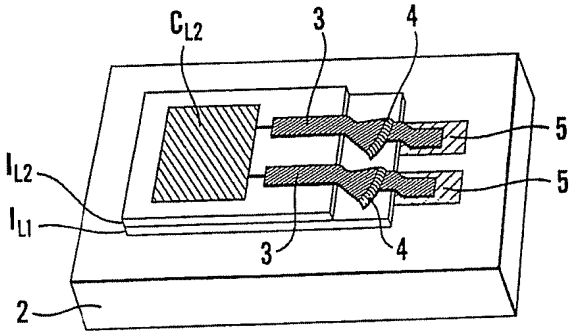


Fig.6c

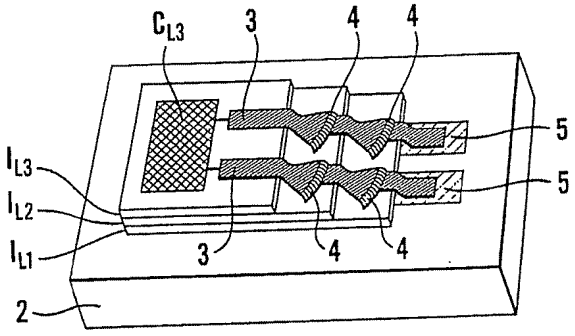
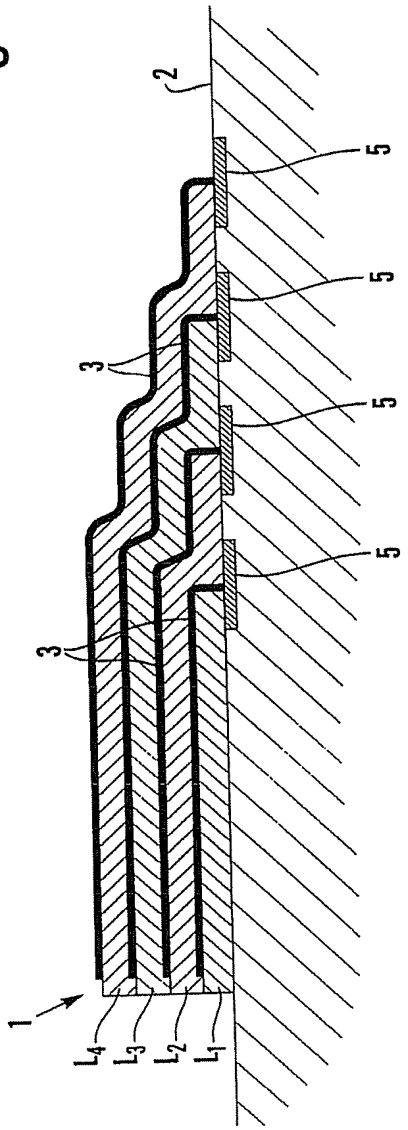


Fig.6d

Fig.7



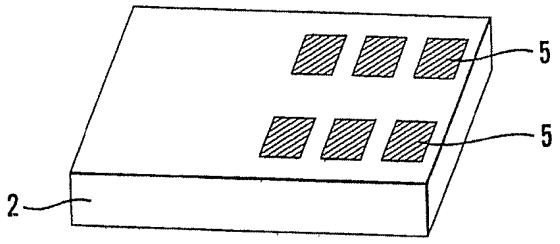
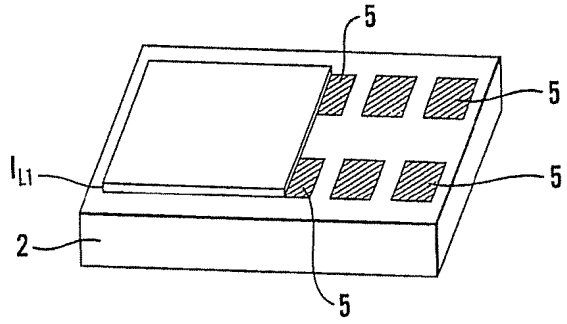


Fig.8a



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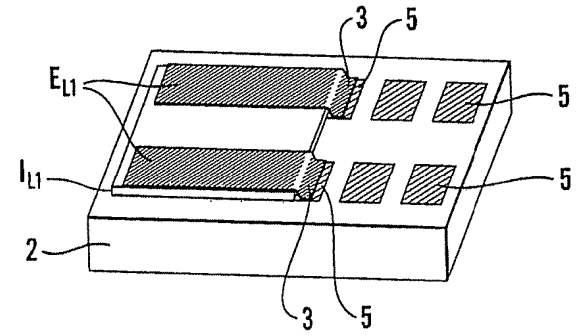


Fig.8c

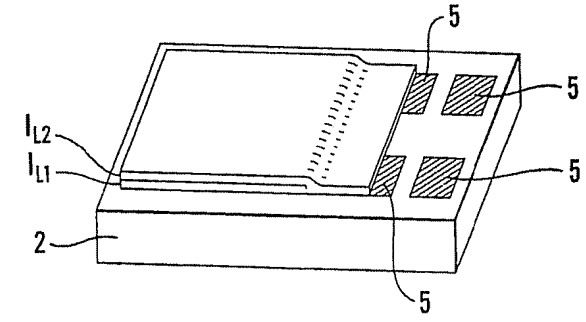


Fig.8d

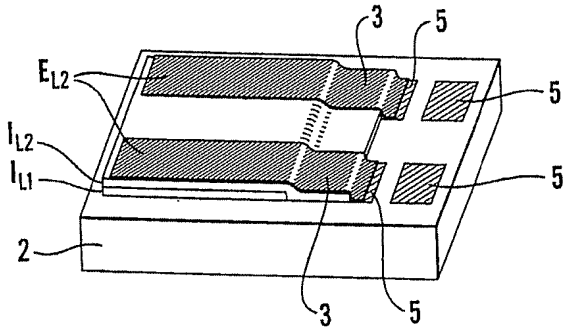


Fig.8e

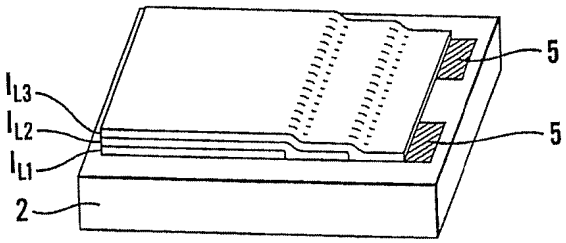


Fig.8f

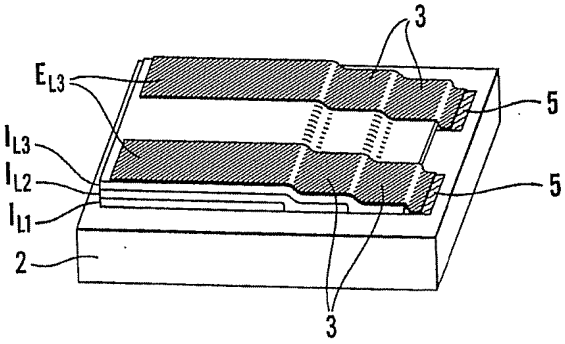


Fig.8g

Fig.9a

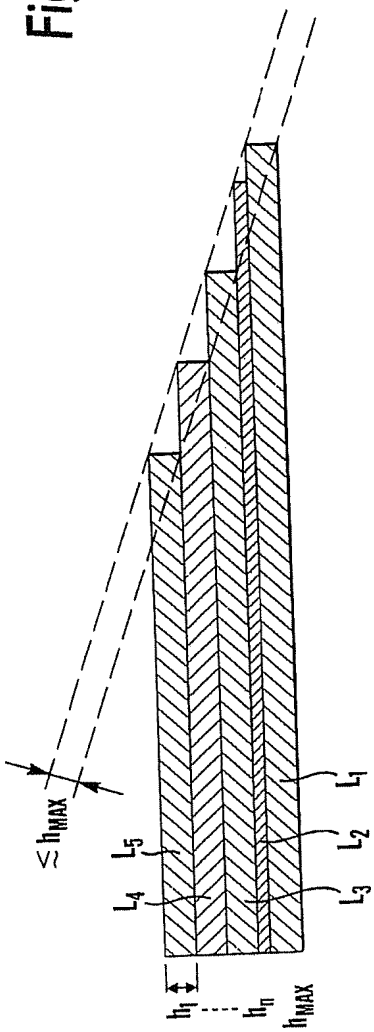
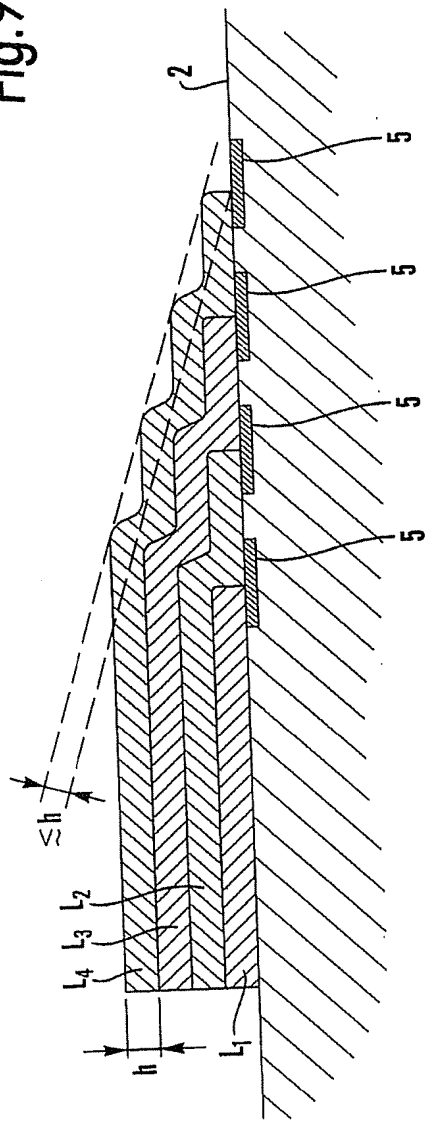


Fig.9b



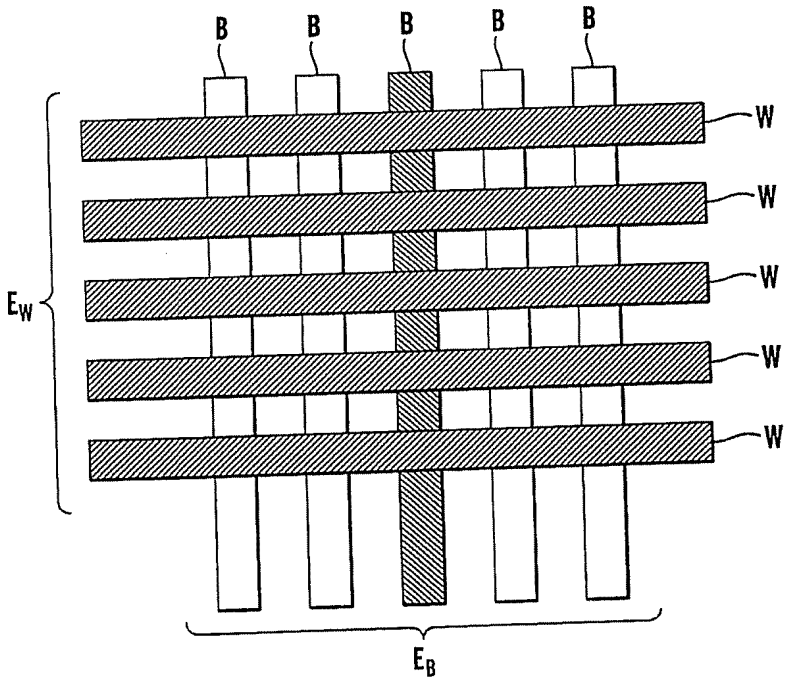


Fig. 10

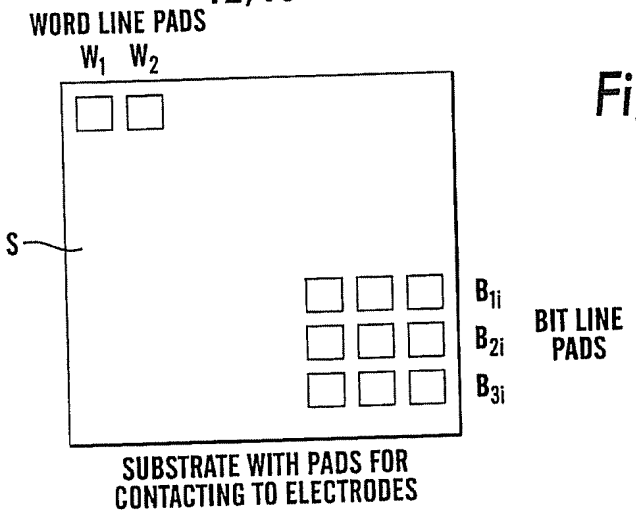


Fig.11a

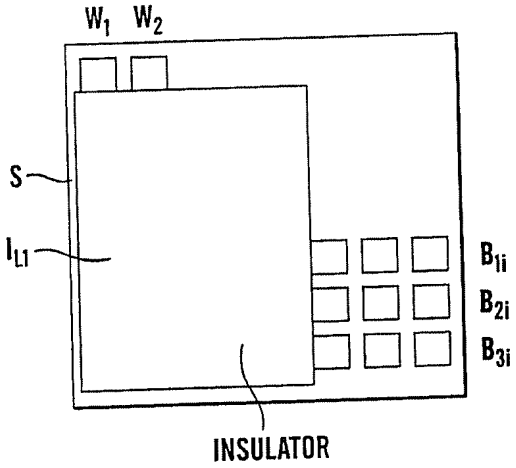


Fig.11b

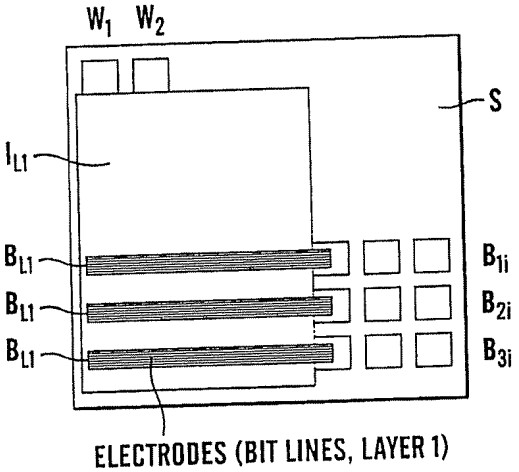


Fig.11c

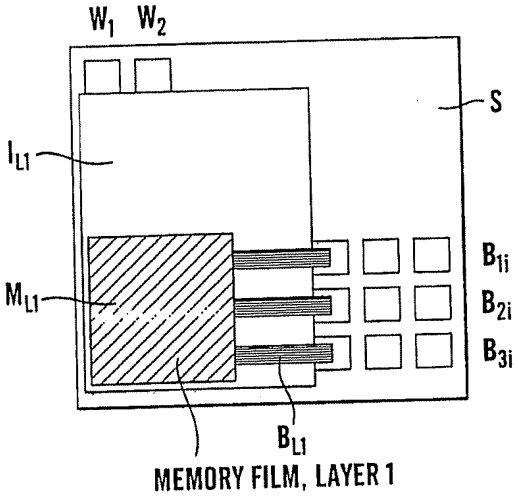


Fig.11d

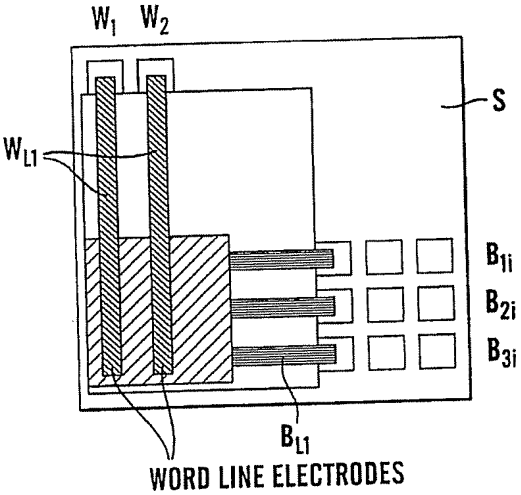


Fig.11e

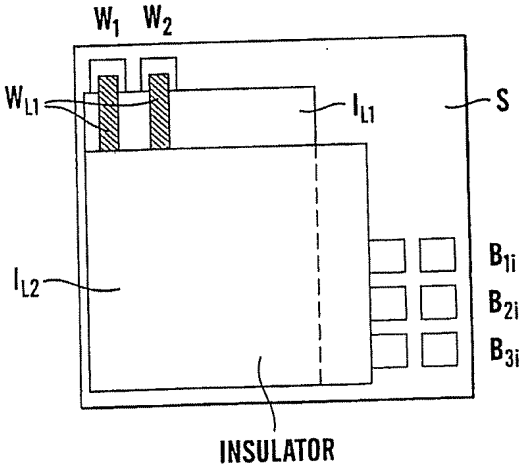


Fig.11f

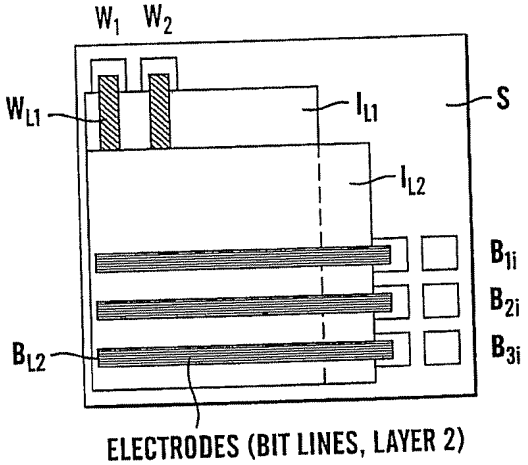


Fig.11g

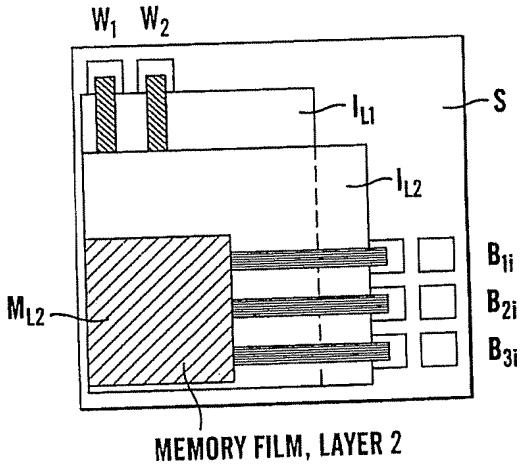


Fig.11h

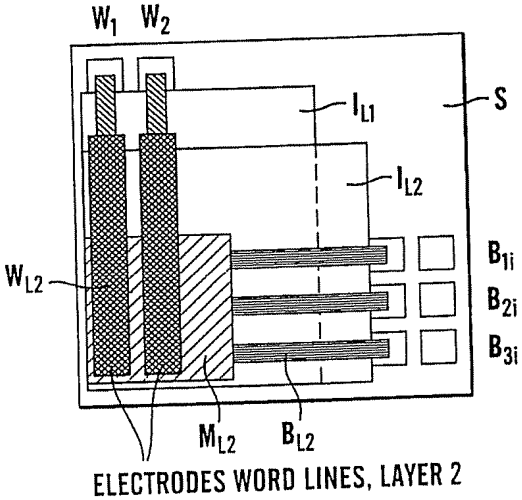


Fig.11i

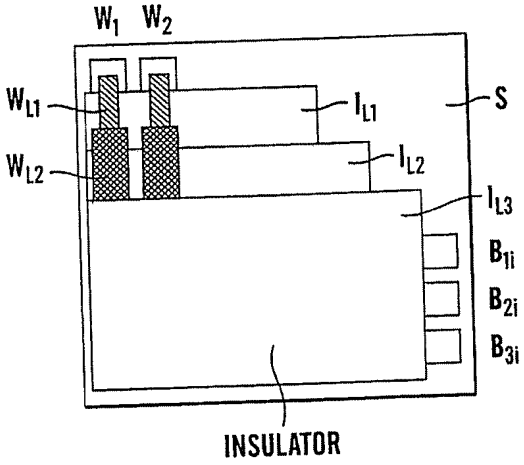


Fig.11j

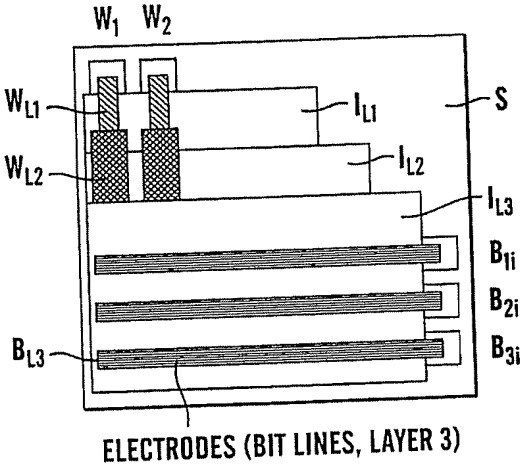


Fig.11k

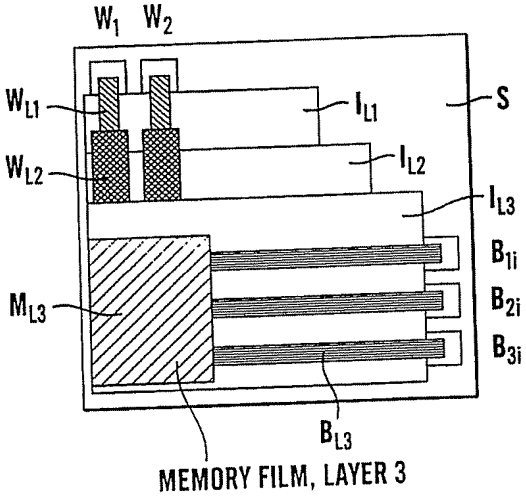
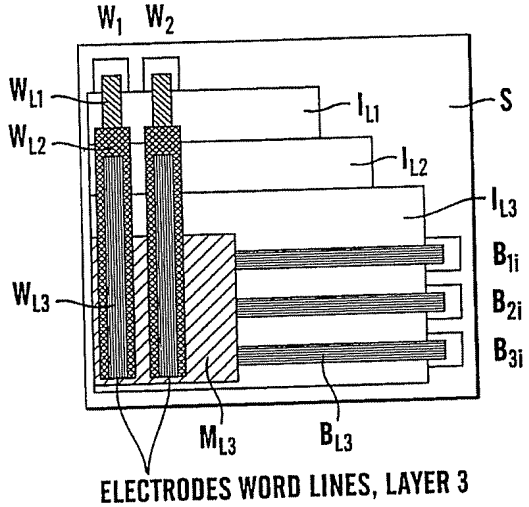


Fig.11l


W1 W2
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WL2
WL3
IL1
IL2
IL3
S
B1i
B2i
B3i
ML3
BL3
ELECTRODES WORD LINES, LAYER 3

Fig. 11m

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 01/00113

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H01L 23/522, H01L 21/60
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H01L, H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5093708 A (ALLEN L. SOLOMON), 3 March 1992 (03.03.92), column 2, line 3 - line 61; column 5, line 65 - column 6, line 16, figure 7, abstract --	1-7
A	US 5502289 A (HEM P. TAKIAR ET AL), 26 March 1996 (26.03.96), figures 6,8, abstract --	1-7
A	EP 0522518 A2 (HUGHES AIRCRAFT COMPANY), 13 January 1993 (13.01.93), figure 3, abstract --	1-7

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2001	21 -06- 2001
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Stig Edhborg/MN Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 01/00113

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Patent Abstracts of Japan, abstract of JP 58-178547 A (MATSUSHITA DENKI SANGYO K.K.), 20 January 1984 (20.01.84), Vol. 8, No. 13 (E222) -- --------	1-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

30/04/01

International application No.
PCT/NO 01/00113

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 5502289 A	26/03/96	DE 69325749 D,T	17/02/00
		EP 0575051 A,B	22/12/93
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